Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-27. (Canceled)

28. (Withdrawn) A method for fabricating a conductive plate with isolated feedthroughs comprising the steps of:

providing a suitable base material for said conductive plate such as copper, or an alloy of copper, or a dispersion hardened form of copper;

drilling said plate with holes on a suitable grid;

filling each of said holes with a plug of dielectric material and polishing to planarize;

drilling said dielectric plugs to create apertures concentric with said holes;

laminating a sheet of dielectric material so as to cover said apertures on one side of said conductive plate;

coating the side and bottom walls of said apertures with an adhesion layer such as titanium, followed by a seed layer of copper;

electroplating copper to fill said apertures and form feedthroughs;

polishing to planarize said electroplated copper and provide electrical isolation between said feedthroughs;

patterning a mask layer of material such as aluminum on said laminated dielectric material, with apertures matching said apertures in said dielectric plugs;

dry etching through said apertures to expose said electroplated copper;

depositing an adhesion layer of a material such as titanium and a seed layer of copper or gold onto said exposed electroplated copper; and,

electroplating said seed layer to produce a plated contact under each of said feedthroughs.

29. (Withdrawn) A dual damascene method for patterning a pair of layers including a conductive layer and a dielectric layer of an interconnection circuit comprising the steps of:

providing a planarized surface with exposed contact pads;

providing a layer of thermoplastic dielectric material over said planarized surface;

aligning a toolfoil and imprinting a dual level pattern, said dual levels including a lesser depth for trenches, and a greater depth for vias, with said vias aligned with said contact pads;

removing any remaining web of dielectric material to expose said contact pads;

coating said imprinted pattern with an adhesion layer of a material such as titanium followed by a seed layer of copper;

electroplating said seed layer to fill said vias and provide a suitable trench thickness of several microns; and,

polishing said electroplated material to provide a planarized surface and to provide electrical isolation between said trenches.

30. (Withdrawn) A method for imprinting a special assembly layer that includes a conductive well at each input/output pad of an interconnection circuit comprising the steps of:

providing exposed input/output pads at a polished and planarized surface;

providing a layer of thermoplastic material over said interconnection circuit;

aligning an embossing tool to alignment features of said interconnection circuit;

pressing said embossing tool into said imprintable dielectric to form a well including at least a portion of said well that is formed in close proximity to corresponding said input/output pad;

cooling to room temperature if necessary and separating said embossing tool from said interconnection circuit;

removing by etching or other means a remaining web of said imprintable material if any, to expose said input output pads;

depositing a diffusion barrier material such as nickel to a thickness of approximately 1.5 microns;

polishing until a planarized surface is achieved and said wells are electrically isolated from one another; and,

filling said wells with solder paste.

31. (Withdrawn) A method for reworking defective die on a blade substrate comprising the steps of:

providing wells filled with solder at input/output pads of said blade substrate;

providing integrated circuits in bare die form;

providing conductive bumps at bonding sites of said integrated circuits, said bonding sites corresponding with said input/output pads;

assembling said integrated circuits onto said blade substrate by inserting said conductive bumps in said wells filled with solder, melting said solder as required;

providing means to test said blade substrate and identify any defective integrated circuits;

heating said blade substrate to a temperature below the solder melting point using a hot plate;

providing additional heat to said defective integrated circuit using hot inert gas applied to the backside of said bare die;

removing said defective integrated circuit by withdrawing said conductive bumps from said wells filled with solder;

cleaning the surface of said blade substrate around the site of said defective die as required;

providing additional solder in said wells as required; and,

inserting a good integrated circuit to replace said defective integrated circuit, providing heating to melt said solder and cooling as required.

32. (Withdrawn) A supercomputer arranged in the approximate shape of a cube comprising:

a parallel array of planar shaped cooling chambers;

blade components, each having a conductive substrate, wherein said substrate is thermally coupled to at least one of said cooling chambers and said blade components each include more than 100 flip chip mounted integrated circuit chips assembled onto circuits fabricated on said substrate.

33. (Withdrawn) The supercomputer of claim 32 wherein said blades are interconnected using blade access cables attached to blade access ports provided on each of said blades.

34. (Withdrawn) The supercomputer of claim 33 wherein each of said blade access ports includes an array of terminals wherein each of said terminals comprises a well filled with solder, and said wells are spaced apart with a pitch of 200 microns or less.

35. (Withdrawn) A blade access cable comprising:
a rigid carrier for use during fabrication;
a release layer employing ultra violet release materials;
one or more signal layers;
two or more ground or power planes; and,
a stud bump at each input/output pad.

36. (Withdrawn) The blade access cable of claim 35 wherein said stud bumps are provided at a pitch of less than 200 microns.

37. (Canceled)

38. (Currently Amended) The interconnection circuit board of Claim 40~~37~~ wherein the copper substrate is fabricated with electrically isolated conductive feedthroughs therein.

39. (Currently Amended) The interconnection circuit board of Claim 38 wherein at least some of the conductive feedthroughs electrically connect with at least some of the plurality of copper traces.

40. (Currently Amended) An interconnection circuit board for use with electronic components comprising:
a copper substrate;

a first dielectric layer on the copper substrate;

a plurality of distinct copper traces on the first dielectric layer;

a second dielectric layer on the copper traces and defining sidewalls of at least a first well having a bottom formed by at least one of the plurality of copper traces ;

a plurality of terminals electrically connected to the respective plurality of copper traces and adapted to permit electrical communication with the electronic components, ~~The interconnection circuit board of Claim 37 wherein~~ at least one of the plurality of terminals ~~includes~~ including a conductive layer on the sidewalls of the at least a first~~a~~ well ~~provided in the underlying dielectric layer~~ and ~~formed by conductive walls disposed on the dielectric layer, the well being substantially filled with~~ conductive material substantially filling the at least a first well.

41. (Currently Amended) An electronic module comprising:

a copper substrate;

a first dielectric layer ~~formed atop~~ on the copper substrate;

~~a copper trace layer having~~ a plurality of distinct copper traces ~~disposed atop~~ on the first dielectric layer;

a second dielectric layer on the copper trace layer, the second dielectric layer defining sidewalls of at least a first well, the bottom of the well formed by at least one copper trace;

terminals ~~provided at ends of at least some of~~ electrically connected to the respective copper traces for permitting electrical communication with the electronic components, at least one of the terminals including a conductive layer on the sidewalls of the well and conductive material substantially filling the well; ~~and~~,

an electronic component attached to the at least one terminal ~~of the terminals~~.

42. (Previously Presented) The electronic module of Claim 41 wherein the copper substrate is fabricated with electrically isolated conductive feedthroughs therein.

43. (Previously Presented) The electronic module of Claim 41 wherein the electronic component includes an integrated circuit chip.

44. (Previously Presented) The electronic module of Claim 41 wherein the electronic component includes a cable.

45. (Previously Presented) The electronic module of Claim 41 wherein the electronic component includes a wireless transceiver chip.

46. (Currently Amended) The electronic module of Claim 41 further comprising an additional electronic component attached to another of the plurality of terminals.

47. (Previously Presented) The electronic module of Claim 41 further comprising a copper top plate attached to a back face of the electronic component.

48. (Previously Presented) The electronic module of Claim 41 further comprising a chamber attached to a back face of the electronic component and adapted for circulating a coolant fluid.

49. (New) The interconnection circuit board of Claim 40 wherein the conductive layer on the sidewalls is formed of a material different than the conductive material substantially filling the at least a first well.

50. (New) The interconnection circuit board of Claim 40 wherein the conductive layer on the sidewalls includes nickel and the conductive material substantially filling the well includes a solder paste.

51. (New) The interconnection circuit board of Claim 41 wherein the electronic component includes a conductive member protruding from the component and extending into the well for attaching the electronic component to the at least one terminal.

52. (New) The interconnection circuit board of Claim 51 wherein the conductive member includes a gold stud bump.

53. (New) The electronic module of Claim 41 wherein the conductive layer on the sidewalls comprises a different material than the conductive material substantially filling the well.

54. (New) The electronic module of Claim 41 wherein the conductive layer on the sidewalls includes nickel and the conductive material substantially filling the well includes solder paste.

55. (New) The electronic module of Claim 41 wherein the second dielectric layer defines a plurality of the wells, each of the wells having a bottom formed by at least one of the conductive traces, each of the terminals comprising conductive material on the sidewalls of a respective one of the wells and conductive material substantially filling each of the wells, the electronic component including a plurality of extending conductive members, the electronic component aligned to the plurality of wells such that the extending conductive members are disposed in the plurality of wells to form an electrical attachment.